Listing of Claims:

This listing of claims reflects all claim amendments and replaces all prior versions, and listings, of claims in the application (material to be inserted is in **bold and underline**, and material to be deleted is in ~~strikeout~~ or (if the deletion is of five or fewer consecutive characters or would be difficult to see) in double brackets [[ ]].

1. (Previously presented) A method of forming an electrically conductive element in an integrated circuit, the method comprising:

depositing a composite polymer dielectric film onto a substrate, wherein the composite polymer dielectric film includes a silane-containing adhesion promoter layer formed on the silicon-containing substrate, and a low dielectric constant polymer layer formed on the adhesion promoter layer, wherein the adhesion promoter layer is at least partially formed from at least one material having a general structure of $(RZ)_x$-Si-$(W\text{-}T)_y$, wherein W is selected from -O-, -CH_2-, -$(CH_2)_a$C=OO-, and -$(CH_2)_a$-OO=C-; wherein T is selected from -CR=CR'R", alkyl chlorides, alkyl bromides, alkyl iodides, and -RC=O; wherein Z is selected from O and NR; wherein R, R' and R" are an H, alkyl or aromatic group; wherein a is 0 or an integer; wherein x = 1, 2 or 3; wherein y = 1, 2 or 3; and wherein x + y = 4;

depositing a silane-containing hard mask layer onto the composite polymer dielectric film;

exposing the hard mask layer and the adhesion promoter layer to a free radical-generating energy source to chemically bond the adhesion promoter layer to the underlying silicon-containing substrate and to the low dielectric constant polymer layer, and to chemically bond the composite polymer dielectric film to the hard mask layer;

etching an etched feature in the hard mask layer and the composite polymer dielectric

film; and

depositing an electrically conductive material in the etched feature.

2. (Previously presented) The method of claim 1, wherein the hard mask layer is formed from at least one material having the general structure of $(RZ)_x$-Si-$(W\text{-}T)_y$.

3. (Original) The method of claim 2, wherein the hard mask layer is formed from an organosilane having a general formula (RZ)-Si-$(W\text{-}T)_3$.

4. (Previously presented) The method of claim 1, wherein the adhesion promoter layer and the hard mask layer are each formed from at least one material having a general structure of H_xSi-$(W\text{-}T)_y$.

5. (Original) The method of claim 1, wherein the low dielectric constant polymer layer is formed from a poly(paraxylylene)-based polymer.

6. (Original) The method of claim 1, further comprising forming a silane-containing barrier layer over the hard mask layer, forming a second low dielectric constant polymer layer over the barrier layer, forming a silane-containing etch stop layer over the second low dielectric constant polymer layer, and exposing the barrier layer and the etch stop layer to the free radical-generating energy source to cause the etch stop layer and the barrier layer to chemically bond to the second low dielectric constant polymer layer.

7. (Previously presented) The method of claim 6, wherein the etch stop layer is formed from at least one organosilane having a general formula $(RZ)_3$-Si-(W-T).

8. (Original) The method of claim 6, further comprising forming a third low dielectric constant polymer layer over the etch stop layer.

9. (Original) The method of claim 8, further comprising forming a second hard mask layer over the third low dielectric constant polymer layer.

10. (Previously presented) The method of claim 9, wherein exposing the hard mask layer and the adhesion promoter layer to a free radical-generating energy source includes simultaneously exposing the hard mask layer and the adhesion promoter layer to a free radical-generating energy source.

11. (Original) The method of claim 10, further comprising:

etching a via through the third low dielectric constant polymer layer, the etch stop layer, and the second low dielectric constant polymer layer;

etching a trench through the third low dielectric constant polymer layer, wherein the trench at least partially overlaps the via; and

depositing an electrically conductive material in the via and the trench.

12. (Original) The method of claim 11, further comprising removing electrically

conductive material from surfaces adjacent the trench via chemical-mechanical polishing.

13. (Original) The method of claim 1, wherein exposing the adhesion promoter layer and the hard mask layer to a free radical-generating energy source includes heating the adhesion promoter layer and the hard mask layer.

14. (Original) The method of claim 13, wherein the composite polymer dielectric film and the hard mask layer are heated under a mixture of hydrogen and a noble gas.

15. (Original) The method of claim 1, wherein exposing the adhesion promoter layer and the hard mask layer to a free radical-generating energy source includes exposing the adhesion promoter layer and the hard mask layer to a UV light source.

16-24. (Canceled)

25. (Previously presented) In an integrated circuit, a method of forming an electrical connection to an underlying electrically conductive element, wherein the electrically conductive element is disposed within a first polymer dielectric film, the method comprising:

forming a second polymer dielectric film over the electrically conductive element and the first polymer dielectric film, wherein the second polymer dielectric film has a composite structure including a first silane-containing adhesion promoter layer chemically bonded to a first low dielectric constant polymer layer, wherein the first adhesion promoter layer is formed from at least one material having a general structure of $(RZ)_x$-Si-$(W\text{-}T)_y$, wherein W is selected from -O-, $-CH_2-$, $-(CH_2)_aC{=}OO-$, and $-(CH_2)_a-OO{=}C-$; wherein T is selected from -CR=CR'R", alkyl chlorides, alkyl bromides, alkyl iodides, and -RC=O; wherein Z is selected from O and NR; wherein R, R' and R" are an H, alkyl or aromatic group; wherein a is 0 or an integer; wherein x = 1, 2 or 3; wherein y = 1, 2 or 3; and wherein x + y = 4;

forming an etch stop layer over the second polymer dielectric film;

forming a third polymer dielectric film over the etch stop layer;

forming a hard mask layer over the third polymer dielectric film;

etching a via through the third polymer dielectric film, the etch stop layer, and the second polymer dielectric film to expose the electrically conductive element;

etching a trench through the third polymer dielectric film such that the trench at least partially overlaps the via; and

depositing an electrically conductive material in the via and the trench, wherein the electrically conductive material contacts the electrically conductive element in the first polymer dielectric layer.

26. (Original) The method of claim 25, wherein the third polymer dielectric film includes a second silane-containing adhesion promoter layer and a second low dielectric constant polymer layer.

27. (Previously presented) The method of claim 25, wherein the etch stop layer is formed from an organosilane material having the general structure of $(RZ)_x$-Si-$(W\text{-}T)_y$.

28. (Previously presented) The method of claim 27, wherein the etch stop layer is formed form an organosilane material having a general structure of $(RZ)_3$-Si-(W-T).

29. (Canceled)

30. (Previously presented) The method of claim 25, wherein the hard mask layer is formed from an organosilane material having the general structure of $(RZ)_x$-Si-$(W\text{-}T)_y$.

31. (Original) The method of claim 30, wherein the organosilane material has a general structure of (RZ)-Si-$(W\text{-}T)_3$.

32. (Original) The method of claim 25, further comprising exposing the second polymer dielectric film to a free radical-generating energy source to chemically bond the first adhesion promoter layer to the first low dielectric constant polymer layer before depositing the third polymer dielectric layer.

33. (Original) The method of claim 32, further comprising exposing the etch stop layer to a free radical-generating energy source to chemically bond the etch stop layer to the first low dielectric constant polymer layer.

34. (Original) The method of claim 33, further comprising exposing the third polymer dielectric film to the free radical-generating energy source to chemically bond the third polymer dielectric film to the etch stop layer.

35. (Original) The method of claim 34, further comprising exposing the hard mask layer to the free radical-generating energy source to chemically bond the hard mask layer to the third polymer dielectric layer.

36. (Original) The method of claim 25, wherein the third polymer dielectric layer includes a second adhesion promoter layer and a second low dielectric constant polymer layer, further comprising exposing the third polymer dielectric layer to a free radical-generating energy course to chemically bond the second adhesion promoter layer to the second low dielectric constant polymer layer.

37. (Original) The method of claim 25, further comprising annealing the via and the trench in a reducing atmosphere before depositing the electrically conductive material in the via and the trench.

38. (Original) The method of claim 37, wherein the via and the trench are annealed in a mixture of hydrogen in a noble gas.

39-50. (Canceled)